640×512 MWIR FPA Detector Module (15μm)

(C308F Stirling Cooler)

Technical Specification

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Technical Specification

1 Overview

The 640×512 MWIR FPA detector module (hereinafter referred to as the "detector module") has the function of converting infrared radiation signals in 3~
5u m wave band into electrical signals. All mechanical, optical and electrical
interfaces are of universality, and can be used in various military and civilian thermal imaging systems such as various night vision equipment, panoramic searching, thermal image sighting, forward looking warning, weapon guidance, air defense monitoring, infrared recognition, infrared diagnostic testing and temperature measurement.

This Specification describes the configuration, performance, features, and detailed operation and maintenance instructions of the detector module.

2 Main Technical Characteristics

a) Array scale: 640×512 (pixel)
b) Pitch: 15μm
c) Power Supply: 3.3V
d) Snap-shot mode, integration then readout (ITR), integration while readout (IWR)
e) Input polarity: N on P
f) Charge capacity: 6.8 Me^- (ITR), 5.5 Me^- (IWR)
g) Output channels: 4
h) Multi-mode and windowing mode readout
i) Direct injection, anti-bloom function
j) Readout rate: Max 10MHz
k) Full frame rate up to 120Hz (640×512)
l) Dynamic range: ≥80dB
m) Power consumption: ≤50mW (without the cooler)

3 Product Configuration, Structure and Operating Principle

3.1 Product configuration

The 640×512 MWIR FPA detector module mainly consists of the following:

a) 640×512 HgCdTe FPA detector chip

b) 640×512 CMOS ROIC

c) C308F integrated Stirling cooler

d) Micro dewar

e) Infrared window

3.2 Product structure

The 640×512 MWIR FPA detector module consists of HgCdTe film material, ROIC, detector chip, micro dewar and C308F integrated Stirling cooler, as shown in Fig. 1.

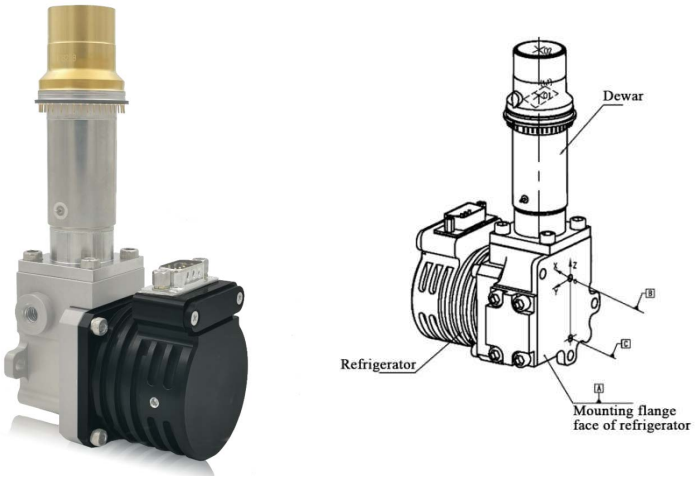


Fig. 1 Configuration Schematic of the 640×512 MWIR FPA Detector Module

3.3 Operating Principle

3.3.1 Configuration of infrared FPA detector chip assembly

The detector chip and the ROIC are interconnected using the advanced flip-chip technology. Indium column arrays with the pitch of 15μm are prepared on the electrodes of the ROIC, and their topological structure is completely consistent with that of the pixels of the detector. The pixels are aligned and bonded with the indium columns one by one using the flip-chip technology to form a hybrid infrared FPA detector. The configuration of the detector chip is shown in Fig. 2.

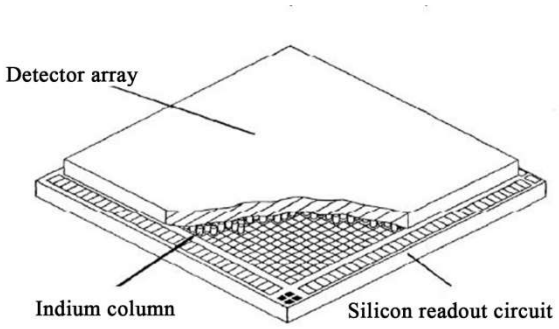


Fig. 2 Schematic Diagram of Flip-Chip Detector Chip Assembly

3.3.2 Detector chip

PV detector chip in the module is fabricated into a 640×512 PV detector array (i.e. consisting of 640×512 PV pixels) on p-HgCdTe by ion implanted junction formation technology.

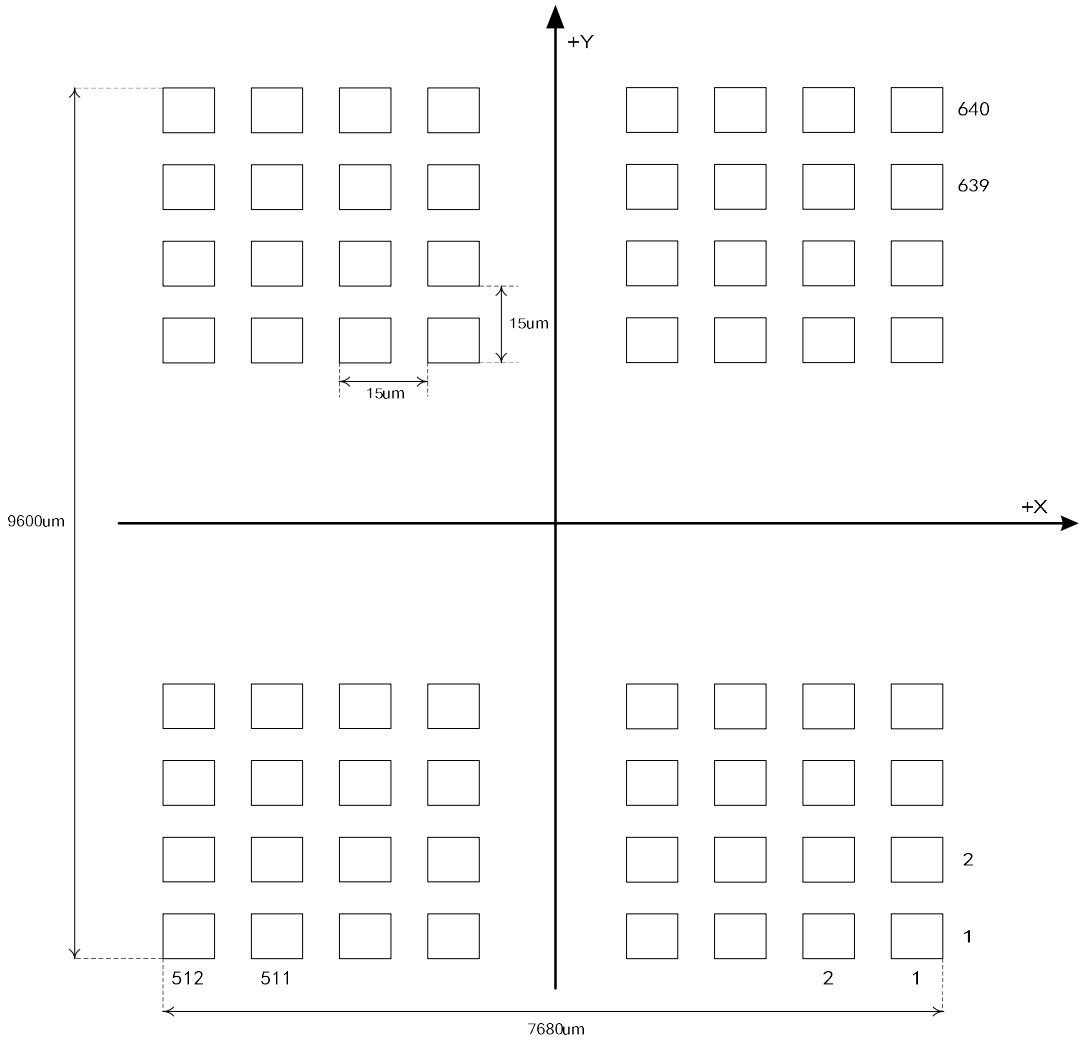


Fig. 3 Topological Schematic of Pixels

3.3.3 Readout integrated circuit

The readout integrated circuit is a 640×512 high-performance snap-shot ROIC. With 640×512, 640×480, 512×512 and windowing mode operation, four outputs, and the unique anti-bloom function of the input stage, it can meet the military or civilian high-precision, high frame rate thermal imaging requirements.

3.3.3.1 ROIC architecture

The ROIC is designed based on the deep submicron silicon CMOS technology, mainly consisting of: input stage (unit pixel) circuit, analog signal processing circuit, digital signal processing circuit, output buffer stage, internal clock generator, internal bias generator, windowing mode circuit, row decoder, column decoder and output unit. The ROIC enables the FPA to integrate, store, pixel select, row select, and sample-hold the instantaneous signal (direct injection) from the photovoltaic diode, using operating mode of integration then readout (ITR) and integration while readout (IWR).

Its architecture is shown in Fig. 4:

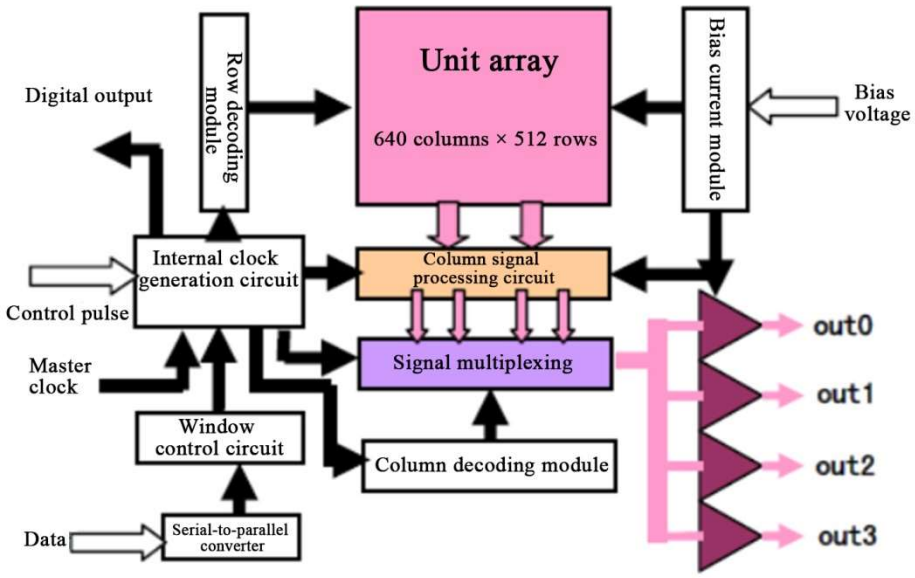


Fig. 4 Schematic Diagram of Functional Module

3.3.3.2 Operating mode

ROIC is designed to have high adaptability, according to the requirements for snapshot operation, users may choose different operating modes, including integration then readout (ITR), integration while readout (IWR), and programmable integration time. See Table 3 for four types of windowing mode.

3.3.3.3 Input stage

The input stage is designed based on the direct injection (DI) principle, with charges stored in the input capacitor within the integration time. The photocurrent signals of PV diode are coupled to the ROIC by direct injection. Integration period starts in the same time at all input stages, integration starts from rising edge and ends at falling edge of "integration signal pulse". i.e. the ROIC operates in the snap shot mode.

3.3.3.4 Charge-Voltage (C-V) conversion and output drive stage

Charges will be converted into voltage upon completion of integration time, and the conversion is completed by the amplifier. Each C-V conversion stage is controlled by the bias voltage generated internally. Four multiplexers (160 to 1) operate simultaneously to send signals from amplifier to four output channels.

There are four output stages, and each output stage corresponds to one multiplexer. The maximum output rate is 10MHz per output channel. The setup time of the output signal is 80ns (the stabilization time is about 15ns with operating frequency of 10MHz). As shown in Fig. 5, the stable time area of the output signal is the sampling area of the signal. Generally, the output signal of the detector needs to be AD converted before digital processing. The sampling point needs to be in the sampling area to ensure the best signal of the detector. Improper sampling points will affect the detector performance.

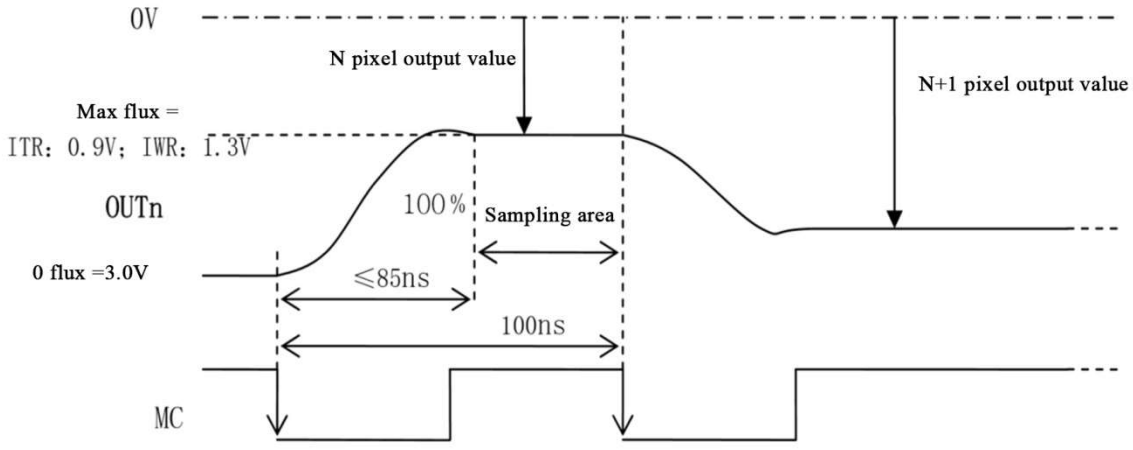


Fig. 5 Schematic Diagram of Output Signal

See Table 1 for output signal dynamic range.

Table 1 Output Signal Dynamic Range

Description	Low level typical value (V)	High level typical value (V)

OUTPUT	0.9(ITR)1.3(IWR)	3.0
DATAVALID	0	3.3
ERROR	0	3.3

3.3.3.5 Time sequence generator and operating time sequence

The time sequence generator generates all the internal signals required by the ROIC through different external clocks and bias voltages. The ROIC operates in a completely synchronous mode. As all the internally generated pulses are an integer multiple of the master clock period, any change of master clock will cause change to these pulses.

The input signals required by the digital control processor are master clock and integration signals:

- Master clock (MC) is the basis of synchronous service of the entire circuit, and has maximum frequency of 10MHz and duty cycle of 50%. Pixel addressing is completed by static synchronous counter controlled by the master clock. Pixel signal is read out by the rate of a period of the master clock.
- The integration signal (INT) allows integration of the charges on the pixel input capacitor (with PV diode biased at high level of INT signal). The integrating capacitor is reset within 3075.5MC cycles after the start of the rising edge of integration (corresponding to the rising edge of MC). Only after this can real charge integration be performed. Therefore, the minimum integration time is 3076.5MC (integration time is 1MC). The integration time can be changed continuously by programming. The falling edge of INT corresponds to the rising edge of MC, and disables the input MOS transistor to end integration.
- Rising and falling time of MC is less than 20ns. To eliminate the fluctuation during integration, INT must be kept stable for 50ns during low level of master clock.

Note: A new calibration (nonuniformity correction) is required after INT change to ensure the acquisition of a satisfactory image.

See Attached Fig. 1-1 for the time sequence chart.

3.3.3.6 Operating mode

3.3.3.6.1 Operating mode selection

ROIC has operating mode of ITR or IWR optional through ITR pin.

Table 2 Operating Mode Selection

Operating mode	Storage capacity
ITR (ITR=1, default)	1.1pC(6.8Me$^-$)
IWR(ITR=0)	0.9pC(5.5Me$^-$)

3.3.3.6.2 Window format selection

Three fixed formats and one windowing mode are optional according to the different input signals SIZEA and SIZEB. SIZEA and SIZEB are used for selecting full window or partial window for each frame. Since SIZEA and SIZEB have instantaneous impact on the digital circuit of the pixel being integrated or the pixel selected for readout, the change to these input signals can only occur between falling edge of DATAVILID and rising edge of INT.

Table 3 Window Operating Mode Selection

SIZEA	SIZEB	Format
1 or suspended	1 or suspended	640×512(default)
1 or suspended	0	640×480
0	1 or suspended	512×512
0	0	Arbitrary windowing mode

In windowing mode, SIZEcol represents the number of pixels in each column of the window (≤512), and SIZEline represents the number of pixels in each row of the window (≤640).

Under different operating modes, the transmission time of the first row of signals in the window to charge-voltage conversion amplifier is respectively:

ITR: 2.5MC+(1/4×SIZEline)×MC;

IWR: The transmission of the first row of signals of frame N-1 starts after 3115.5MC upon rising edge of frame N INT signal, with transmission time of 3115.5MC+(1/4×SIZEline)×MC

DATAVALID output is automatically set to high level, indicating that the first row of signals on the four outputs are valid at the same time (from OUT0 to OUT3). Since there are four outputs, the readout cycle of each row is: (1/4×SIZEline)×MC.

The readout time of the whole window is: 1/4×SIZEline×SIZEcol×MC.

DATAVALID will become 0 after all pixels in selected window are read out.

Before the integration of the next frame, falling edge of DATAVALID **must have interval of at least 1 MC** from rising edge of INT.

In ITR mode, the minimum frame period is: integration time+2.5 MC+1/4× Sizline× MC+1/4× Sizline× Sizecol× MC+1MC.

In IWR mode, the minimum frame period is the larger one between (integration time+1MC) and

(3115.5+1/4×SiZEline+1/4×SIZEline×SIZEcol+1)×MC; and maximum frame frequency is 117.3Hz for 640×512 full frame.

3.3.3.6.3 Windowing control and serial port

In windowing mode, window size is determined by X and Y relative to reference points on the corner. Minimum window size is 132 columns×1 row (640×512).

Possible row width is 132+4×n (0≤n≤127).

Serial data interface has some provisions on coordinates:

See the figure below for position of pixel (0, 0) = (column 1, row 1) given relative to the direction of dewar.

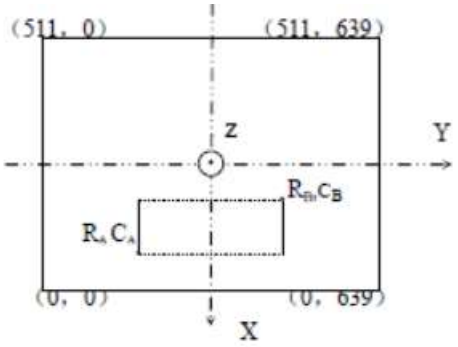


Fig. 6 Windowing Position Diagram

(RA; CA) is the first corner of the window (point A), and (RB; CB) is another relative corner of the window (point B), which are addressed by RMIN, CMIN, RMAX and CMAX.

Window coordinate data (RMIN, CMIN, RMAX and CMAX) are covered in the following input signals: SERCLR and SERDAT, which are sent to IRFPA through serial port. The clock used in windowing logic is master clock MC, which is the same as that used for time sequence.

SERCLR: Falling edge of SERCLR represents the start of serial data SERDAT, and SERCLR must be changed on rising edge and confirmed on falling edge of MC.

SERDAT: Serial data input is allowed. These data are input in specific sequence: RMIN(9bit), RMAX (9bit), CMIN (8bit), CMAX (8bit), starting from maximum weight bit: [RMIN (8)…CMAX (0)], 34 bits.

$R_A = R_{MIN}$ $0 \leqslant R_{MIN} \leqslant 511$

$R_B = R_{MAX}$ $R_{MIN} \leqslant R_{MAX} \leqslant 511$

$C_A = 4 \times C_{MIN}$ $C_{MIN} + 32 \leqslant C_{MAX}$

$C_B = 4 \times C_{MAX} - 1$ $C_{MAX} \leqslant 160$

See Attached Fig. 1-2 for time sequence in windowing mode.

3.3.3.6.4 Windowing operating mode

Window definition data (RMIN, RMAX, CMIN, CMAX) are sent to the first register through serial port. In case of no error (ERROR is low), these data will be loaded into the second register in parallel between falling edge of DATAVALID (end of integration-readout cycle) and the next rising edge of INT. At the beginning of power on, stage-2 parallel register is loaded with 640x512 coordinates. This avoids the unstable state of windowing mode during power on and enables the circuit to immediately turn to normal service.

When ROIC is powered on, parallel register is in uncertain state, thus in windowing mode, the following steps are required to use ROIC:

- Window selection data needs to be sent in through serial port.
- After all the data are sent in, ERROR signal must be tested at low level. In case of error during data input (ERROR turns to high level after all the bits are input), data need to be resent.
- Data will be automatically sent into parallel register on falling edge of DATAVALID.
- The data for the definition of the next window can be sent at any time. In case of no error during transmission, data will be automatically applied to the next integration time and readout cycle upon the end of readout time.

3.3.3.6.5 Rotation function

UPCOL and UPROW are logical inputs that determine the readout direction of the window address. UPROW determines the readout direction of the row and UPCOL determines the readout direction of the column, as shown in Table 4:

Table 4 Rotation function control table

UPCOL	UPROW	Readout direction
1	1	From RA, CA to RB, CB
0	0	From RB, CB to RA, CA
1	0	From RB, CA to RA, CB
0	1	From RA, CB to RB, CA

3.3.3.6.6 Dynamic range

In ITR mode, the maximum charge that can be stored in the ROIC is 1.1pC (6.8Me$^-$), and the dynamic range is 2.1V. In IWR mode, the maximum charge that can be stored in the ROIC is 0.9pC (5.5Me$^-$), and the dynamic range is 1.7V.

3.3.3.7 Relationship between frame rate selection and clock frequency, operating mode and integration time

The maximum frame rate of this detector can reach 120Hz. However, the actual maximum frame rate is determined by the integration time, pixel readout time and detector clock frequency through mutual restriction. As shown in fig. 1-1, the full frame period of the detector is mainly composed of integration capacitor reset time, integration time and pixel readout time.

In ITR mode, the minimum frame period is: integration time $+ 2.5MC + \frac{SIZE_{line} \times MC}{4} + \frac{SIZE_{line} \times SIZE_{col} \times MC}{4} + 1MC$

In IWR mode, the minimum frame period is the larger one between (integration time +1MC) and $3115.5MC + \frac{SIZE_{line} \times MC}{4} + \frac{SIZE_{line} \times SIZE_{col} \times MC}{4} + 1MC$, and the maximum frame rate is 117.3Hz for 640×512 full frame.

For example, the calculation is as follows:

If the master clock of the detector is determined as 10MHz, each clock cycle is $MC = \frac{1}{f} = \frac{1}{10MHz} = 0.1\mu s$.The integration time is set as 4ms according to F2 module. 640×512 full frame output.

In ITR mode, the minimum frame period is $4ms + 0.25\mu s + \frac{640 \times 0.1\mu s}{4} + \frac{640 \times 512 \times 0.1\mu s}{4} + 0.1\mu s \approx 12.2ms$.Theoretical maximum frame rate: $\frac{1}{12.2mS} \approx 82Hz$.At this time, the maximum adjustable integration time is 4ms. If the integration time needs to be increased, the maximum frame rate will be reduced accordingly.

In IWR mode, the minimum frame period is the larger one between $3115.5 \times 0.1\mu s + \frac{640 \times 0.1\mu s}{4} + \frac{640 \times 512 \times 0.1\mu s}{4} + 0.1\mu s \approx 8.5ms$ and the integration time 4ms.Therefore, 8.5ms is taken for calculation, the maximum frame rate is 117.3Hz. At this time, the maximum adjustable integration time is 8.5ms. If the integration time needs to be increased, the maximum frame rate will be reduced accordingly.

It should be noted that in IWR mode, the dynamic range will be reduced from 2.1V in ITR mode to 1.7V. Users need to weigh and consider it in design.

Note：In this section "integration time" include the 3075.5MC.

3.3.4 Stirling cooler

The Stirling cooler provides the infrared detector with the low-temperature operating environment required to ensure the best performance of the infrared detector.

The Stirling cooler is mainly composed of compressor, piston, condenser, cold finger, circuit interface, drive control circuit module, and mechanical reference locating surface. The motor provides power for driving the compressor piston. The regenerator serves as a heat exchanger for conveying and recovering refrigerants in the cooling system. The cold finger is a heat exchange interface of the cooling system, and its working surface, i.e. cooling front end, is the interface for thermal coupling with the detector chip assembly. The detector chip assembly is attached to the front end of the cold finger operating surface of the cooler, to acquire required operating temperature.

The temperature sensor of the Stirling cooler is installed at the front end of the cold finger operating surface, and works with the drive control circuit module to perform closed-loop temperature control. It can control and stabilize the operating temperature of the detector chip assembly at the cooling front end.

3.3.5 Dewar

The dewar is intended to provide reference for mechanical installation and connection of imaging optical system, detector, electronic signal processor and cooler, protect the detector and realize electrical connection, maintain vacuum insulation required for low-temperature operation of the cooler, and to ensure stable operation of the detector in a low-temperature environment.

a) A detector/dewar module is formed by the connection of the dewar with Stirling cooler (see Fig. 1), inner tube of the dewar is matched with the cooler properly. The dewar is equipped with infrared optical window and cold shield, which are necessary for detector module.
b) The dewar is airtight to ensure internal vacuum, activating getter through the activation electrode on the dewar can regularly maintain the vacuum degree required for vacuum insulation.

3.3.6 Infrared optical window

Infrared optical window is made of silicon monocrystal, and the window is coated with infrared antireflective film to limit transmission wavelength range and adjust transmission uniformity, and the window is not transparent to visible light. The infrared window is located at the front end of the dewar, directly facing the detector chip. It is relatively fixed with the detector chip.

The infrared optical window is part of the airtight vacuum system, and also serves as the boundary of the proximity to detector chip for external optical system.

3.3.7 Cold shield

Cold shield is used to suppress background radiation interference, and is composed of multiplestage blackened metal apertures, the diameter of apertures limits field of view of detector, determines maximum F number of an optical system, and is an important optical parameter of detector.

An aperture opening is set on the cold shield to determine the detector's field of view and limit background radiation. The aperture opening of cold shield and the relative distance from the focal plane of detector determine F# (F number), which is an important optical parameter of detector module.

4 Product Performance Parameters and Technical Feature

The general technical parameters of the detector module are described below. Specific product parameters shall be subject to the assignment.

4.1 Performance parameters

The main technical parameters of the detector module are as follows:

Table 5 Main Technical Parameters Requirement

S/N	Main Tactical and Technical Parameters	Parameters Requirement
1	Scale	640×512
2	Pitch	15μm
3	Spectral response range	3.7±0.2μm~4.8±0.2μm
4	Operating temperature	77K~90K
5	Average noise equivalent temperature difference	≤22mK(F1.8/2/3/4)
6	Blind pixel requirement	Blind pixel rate ≤0.5%
7	Non-uniformity of responsivity	≤6%(F1.8/2/3/4)
9	F number	F#=1.8/2/3/4
10	Cooler type	Integrated Stirling cooler
11	Cool down time	7.5min (room temperature: 23±2°C)

4.2 Thermal and Physical Performance

See Table 6 for main thermal and physical performance parameters of detector module.

Table 6 Thermal and Physical Performance parameters of 640×512 FPA Detector Module

Name of parameters	Symbol	Technical Requirement	Unit	Description
Cool down time	Tcd	≤7.5/10	min	Room temperature23±2°C / high temperature 60±2°C
Power consumption	Pcd	≤10/18	W	Temperature regulation/Cool down(Room temperature23±2°C)
Weight	WTIDDCA	≤600	g	Module weight

4.3 Temperature adaptability

The product meets the requirements of temperature characteristic test under the following conditions:

a) High-temperature storage: 48h at +70°C.

b) Low-temperature storage: 24h at -55°C.

c) High-temperature operation: 1h at constant temperature of +60°C and 0.5h under power-on condition.

d) Low-temperature operation: 1h at constant temperature of -40°C and 0.5h under power-on condition.

e) Temperature shock: -56°C~+60°C, with the maximum temperature change rate of ±7°C/min.

4.4 Environmental stress adaptability

4.4.1 Vibration performance

The detector module meets the following testing requirements:

Table 7 Vibration Test Performance

Test Item	Test Conditions	Result and Description
Random vibration	20Hz~80Hz,+3dB/OCT 80Hz~350Hz,0.04g^2/Hz 350Hz~2000Hz,+3dB/OCT (The above conditions are based on 3 axes x, y and z, with 3 min/axis)	The detector module was externally intact without any damage and met various performance requirements.

4.4.2 Shock Performance

The detector module meets the following testing requirements:

Table 8 Shock Test Performance

Test Item	Test Conditions	Result and Description
shock	Back peak sawtooth wave, 30g, 11 ms (apply three shocks in each of the six directions of three mutually perpendicular axes, 18 shocks in total)	It was intact without any damage and still met performance requirements.

4.5 Reliability

a) MTTF≥6000h.

b) Storage lifetime: ≥10 years.

5 Products Supporting and Interconnection Interface Relationship

5.1 Products Supporting

Refer to Table 9 for the whole product set of the 640×512 MWIR FPA detector module.

Table 9 Whole Product Set of the 640×512 MWIR FPA Detector Module

Description	Specifications	Unit	Qty.
Detector module	640×512	Pcs.	1
Window protection cover		Pcs.	1
Test report		Copies	1
Specification		Copies	1

5.2 Interface

5.2.1 Outline dimension drawing

Refer to Attached Fig. 2-1 and Fig. 2-2 for the dimensions of mechanical interfaces of the 640×512 detector module.

5.2.2 Optical interface

The optical interface is an installation interface with the optical system, as shown in Attached Fig. 3.

5.2.3 Electrical interface

The electronic connection interface mainly includes ceramic lead ring interface and vacuum

activation electrode of the detector module. Refer to Attached Fig. 4 for the ceramic lead ring interface of the detector module.

5.2.4 Cooler controller interface

The cooler adopts DC input mode with voltage of 24V ± 1V. Refer to Attached Fig. 5 for cooler controller interface.

5.2.5 Circuit interface of detector module

The circuit interface of the detector module is a 41-pin ceramic lead ring, with specific functions and requirements shown in Tables 10 and 11. The pin functions include:

a) 9-channel analog input (provided by external drive circuit).
b) 9-channel digital input (provided by external drive circuit).
c) Output end of 4-channel output signal.
d) 2 independent temperature sensors.
e) Pin A11 is connected with the dewar shell, and the insulation resistance between other pins and the shell is ≥1 MΩ (measured by a digital multimeter, with the black probe connected to the shell).

The pins marked with "NC" are generally suspended. In case of high system noise, a jumper can be used for selective short circuiting with the analog ground or digital ground. Generally, COLDSHIELDGROUNG is short circuited with the analog ground. DEWARGROUND is short circuited with the system shell or suspended. During the design, if the PCBs on sides A and B are not the same one, they shall be short-circuited with the ground wire nearby to reduce system noise or interference.

Table 10 Bias Voltage

Description	Bias Type	Voltage Range (V)	Typical Value (V)	Maximum Current	Power Supply Rejection
VDDA analog power supply	Fixed	-	3.3±0.05	<20mA (peak)	-80dB
VDDO analog output power supply	Fixed	3.3~4V	3.6±0.05	<50mA	-55dB
VDDL digital power supply	Fixed	-	3.3±0.3	<30mA	-80dB
GPOL diode bias voltage	Adjustable	0~1.5	0.65±0.05	<2mA	-13dB
VR external bias voltage	Fixed	-	3.0±0.05	<30mA	0dB

VSSA analog electrical GND	Fixed	Ground	0	-	-
VSSL digital electrical GND	Fixed	Ground	0	-	-
VSSO analog output electrical GND	Fixed	Ground	0	-	-
SUBPV PV diode substrate	Fixed	Ground	0	-	-
IBP output current source(20kΩ resistor to GND)(10~30kΩ adjustable)	Fixed		Generated internally		

Table 11 Interface Definition

Description	Definition	Description	Definition
Gpol	Diode bias voltage	MC	Master clock
VDDL	Digital power supply	INT	Integration signal
VSSL	Digital electrical ground	SIZEA	Detector array format
VDDA	Analog power supply	SIZEB	Detector array format
VSSA	Analog electrical ground	UPCOL	Column readout direction
VDDO	Analog output power supply	UPROW	Row readout direction
VSSO	Analog output electrical ground	SERCLR	Input data reset and verification
VR	External bias voltage	SERDAT	Serial data input interface
SUBPV	PV diode substrate	ITR	Input stage operation mode
IBP	(Output current source)	WINDOW_ENA	Windowing control
OUT0/1/2/3	Analog output of detector module	DATAVALID	Digital output, indicating that there is valid output data on OUTPUT
		ERROR	Digital output, indicating serial data input state
The voltage range of all digital drive pulses is 0~3.3V (low if the voltage is <0.6V, and high if the voltage is > 2V)			

5.2.6 Minimum electrical interface of FPA module

Generally, when the ROIC operates in the default mode (minimum electrical interface mode), there are:

a) 10 bias voltages as shown in Table 10.
b) Two pulse voltages MC and INT.

c) Four outputs OUT0~OUT3.
d) DTA and DTK cooler controller interfaces.
e) IBP to ground needs to be connected with 20kΩ resistor(10~30kΩ adjustable).

Note: When SIZEA, SIZEB, SERCLR, SERDAT, UPCOL, UPROW, and ITR inputs are not provided, default value is 3.3V. while default WINDOW_ENA is 0V.

5.2.7 Power consumption of the ROIC

The power consumption of the ROIC is affected by the master clock frequency and output format, and its typical value is ≤50 mW.

5.2.8 Ultimate parameters

The ultimate parameters of the detector chip under normal operation condition are shown in the table below:

Table 12 Ultimate Parameters of the Detector Chip Operating

Description	Definition	Ultimate Value			Unit
		Minimum	Typical Value	Maximum	
VDDA	Analog power supply	3	3.3	3.6	V
VDDO	Analog output power supply	3.2	3.6	3.9	V
VDDL	Digital power supply	3	3.3	3.6	V
GPOL	Diode bias voltage	0	0.65	1.5	V
VR	Internal voltage reference	2.95	3.0	3.05	V
Tj	FPA temperature	/	77	110	K
VOUT	Output voltage range	0	/	3.3	V
R_{LOAD_A}	Analog output load resistance	100k	/	/	Ω
R_{LOAD_D}	Digital output load resistance	10k	/	/	Ω
C_{LOAD_A}	Analog output load capacitance	/	/	15	pF
C_{LOAD_D}	Digital output load capacitance	/	/	80	pF
ESD	Electrostatic protection	/	/	2000	V
D_H	Digital drive high level	2	/	3.6	V

D_L	Digital drive low level	0	/	0.6	V

CAUTION: Only when the temperature is below 100K, the detector chip can be power-on, otherwise performance change or damage caused is not within the scope of warranty.

5.2.9 Temperature sensor interface

Two 2N2222 semiconductor temperature sensors are attached to the cooler front end inside the dewar, and are led out through chip circuit interface of the detector module. The constant current of the sensors is generally set to 0.5 mA. The pins of two temperature sensors at the chip circuit interface of the detector module are A18 (-) and A19 (+), B16 (+) and B17 (-).Commonly two independent temperature sensors are identical, with one for cooler controller feedback and one defined by users.

6 Limitations and Cautions for Use and Maintenance of the Product

6.1 Use and maintenance

6.1.1 Use and operation of the module

Operators shall wear electrostatic-proof gloves and electrostatic-proof wrist straps, The process below shall be followed:

a) Remove the window protective cover and short circuit ring of the detector module.
b) Connect the lead wires of the detector module with the circuit board, and fix the electrical interface of the cooler after connection, to protect the cooler circuit against damage due to falling off during operation.
c) Switch on the cooler power supply, and then power on the detector when the cooler reaches the operating temperature of the detector.

6.1.2 Getter activation

a) Getter activation refers to normal maintenance of the module's vacuum system, and the activation interval shall depend on the actual service environment of users.
b) The getter activation electrode is located at the center of the dewar, and is connected with two getters inside the dewar. The dewar shell serves as a common electrode.

Note: To protect the electrode insulator during getter activation, it is suggested to cool down the activation electrode and the dewar shell with at least 0.4 MPa nitrogen or compressed

air. It is recommended to return to the factory for maintenance, and users are not recommended to handle it by themselves.

6.1.3 Maintenance

The module is a high-tech integrated product. Do not handle any difficult fault at your own discretion. Instead, please consult relevant technicians or the manufacturer's after-sales service department in time for handling opinions.

The module is in a closed state in the infrared application system, so it requires no routine maintenance except vacuum activation when professional personnel considers necessary to do so.

6.2 Troubleshooting

6.2.1 Safety Protection Device and Troubleshooting

Short-circuit ring of the Module serves as electrostatic-proof protector, and must be installed appropriately during release from circuit interface. Please immediately stop operation in case of any abnormal noise and abnormalities during operation.

6.2.2 Fault analysis and troubleshooting

In case of a fault of the module in use, it is necessary to record fault symptom and analyze fault causes.

6.3 Precaution

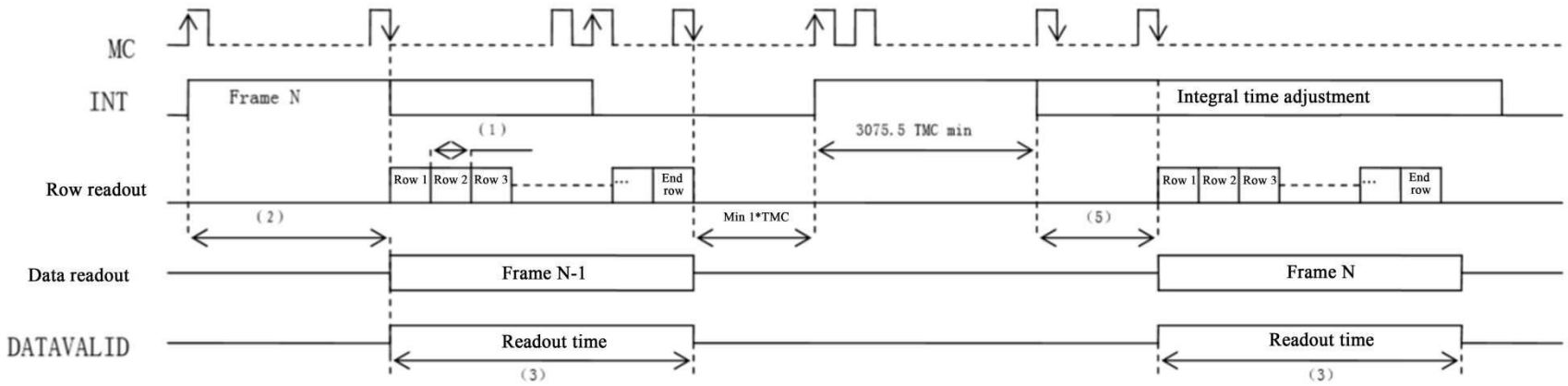
a) The detector module is a device with high-sensitivity integrated circuit. It must be handled with care to avoid collision. Users shall read the technical specification and relevant technical documents in detail before use, and shall receive specialized technical training.
b) The detector module must be equipped with peripheral circuits such as drive circuit and corresponding power supply. The drive circuit includes special interface circuit and low-noise signal adapter circuit (or low-noise preamplifier circuit) matching the chip circuit interface of the detector module.

6.4 Packaging and transportation

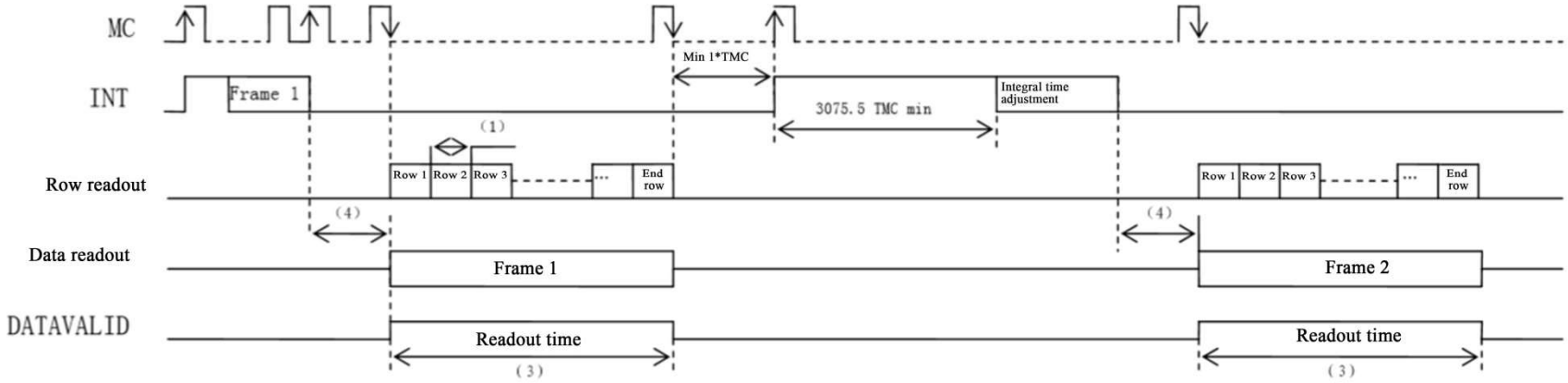
a) The product shall be packaged in a firm packing box for transportation, and shall be transported in the specified manner. The box shall be externally marked with such signs conforming to GB/T191 as "Handle with Care", "Keep Away from Moisture", and "Placement Direction".
b) The product shall be protected against direct exposure to rain , snow and mechanical collision in transit.
c) The product shall be stored properly with reliable special package.
d) The storage environment shall be kept at the temperature of −10°C~40°C, and be kept ventilated and dry without any corrosive gas.

7 Attached Figures

IWR Time Sequence Diagram (ITR=0)



ITR Time Sequence Diagram (ITR=1)

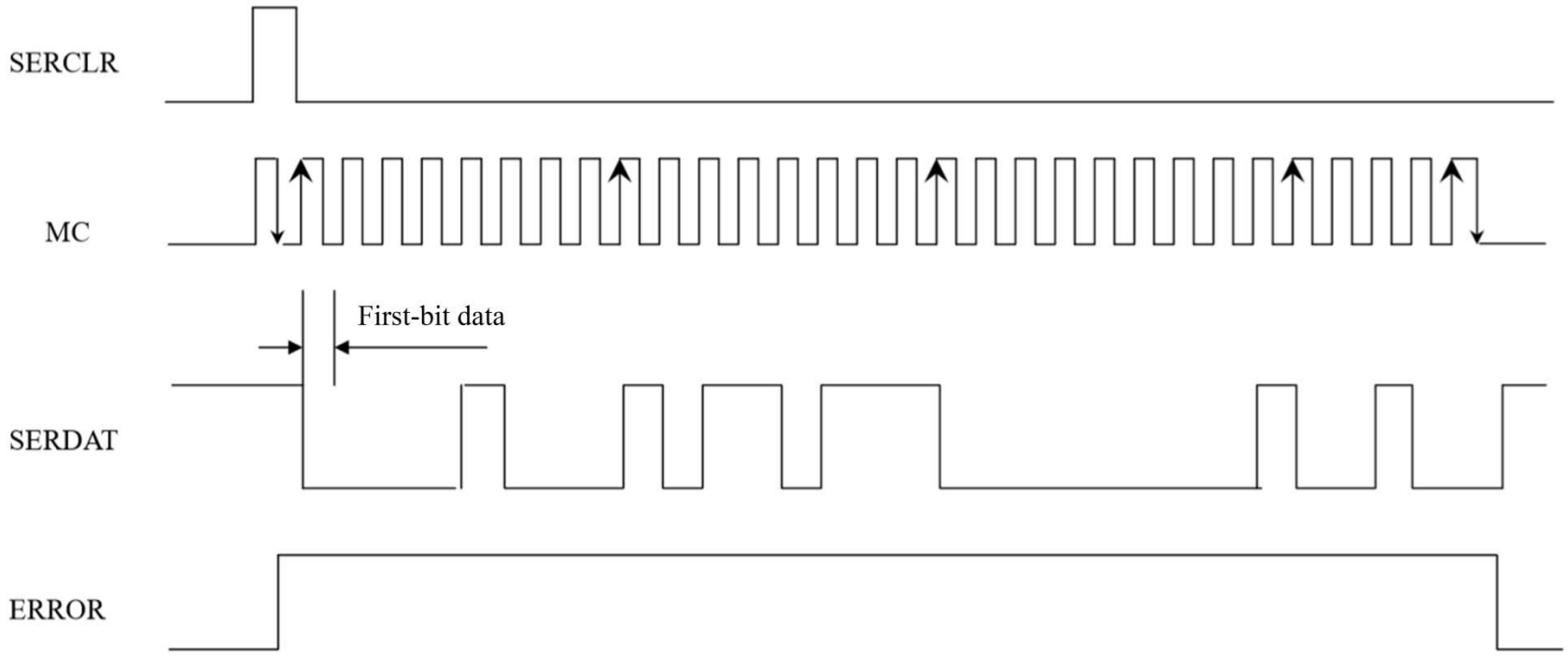


Attached Fig. 1-1 Time Sequence Diagram of ITR and IWR Operation Modes

(1): pixels on one row × TMC/4　　(2)：3115.5×TMC+（1）　　(3): pixels on one row × rows of each frame × TMC/4

(4)：2.5×TMC+（1）　　(5)：40×TMC+（1）

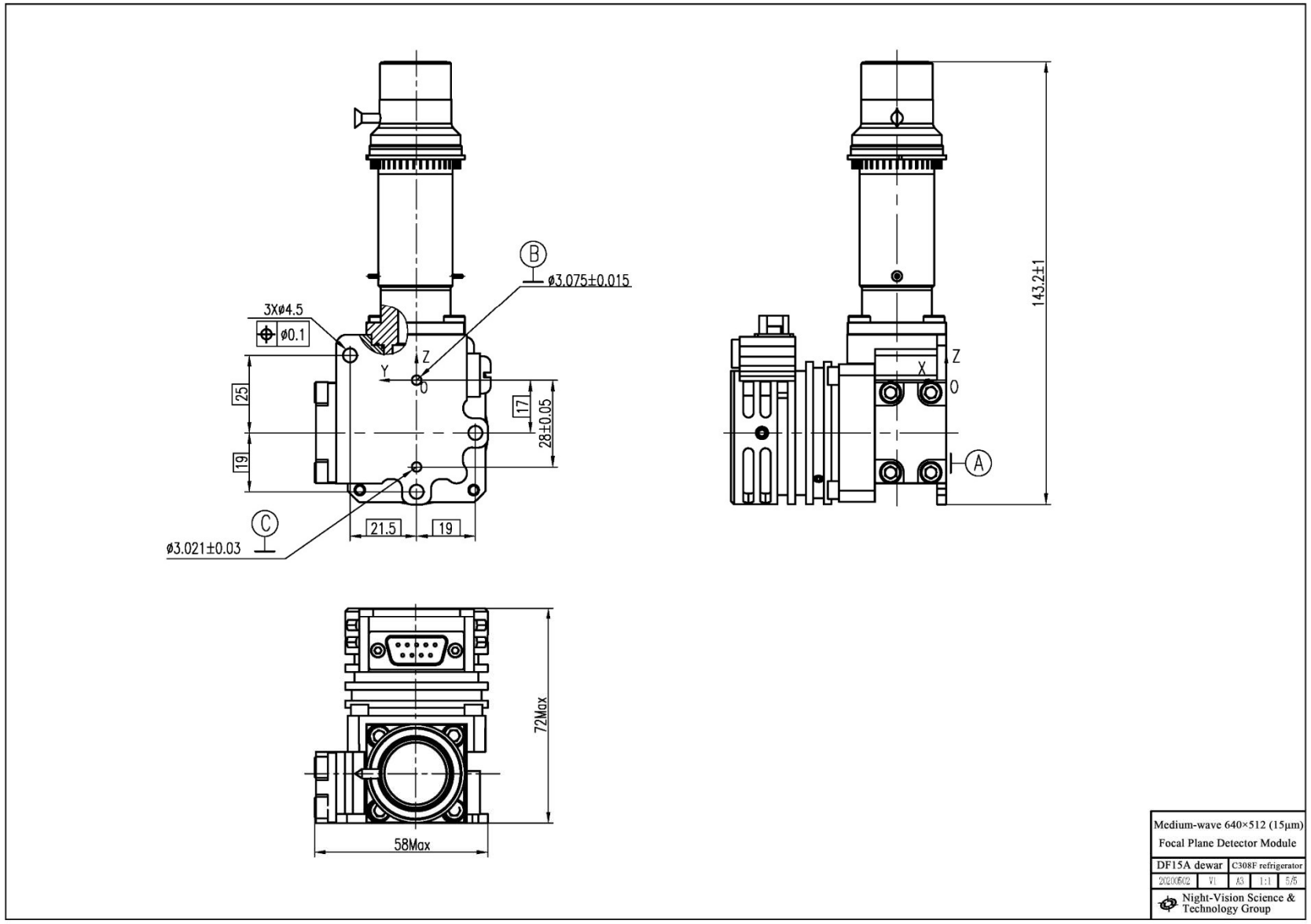
When WINDOW ENA=1:



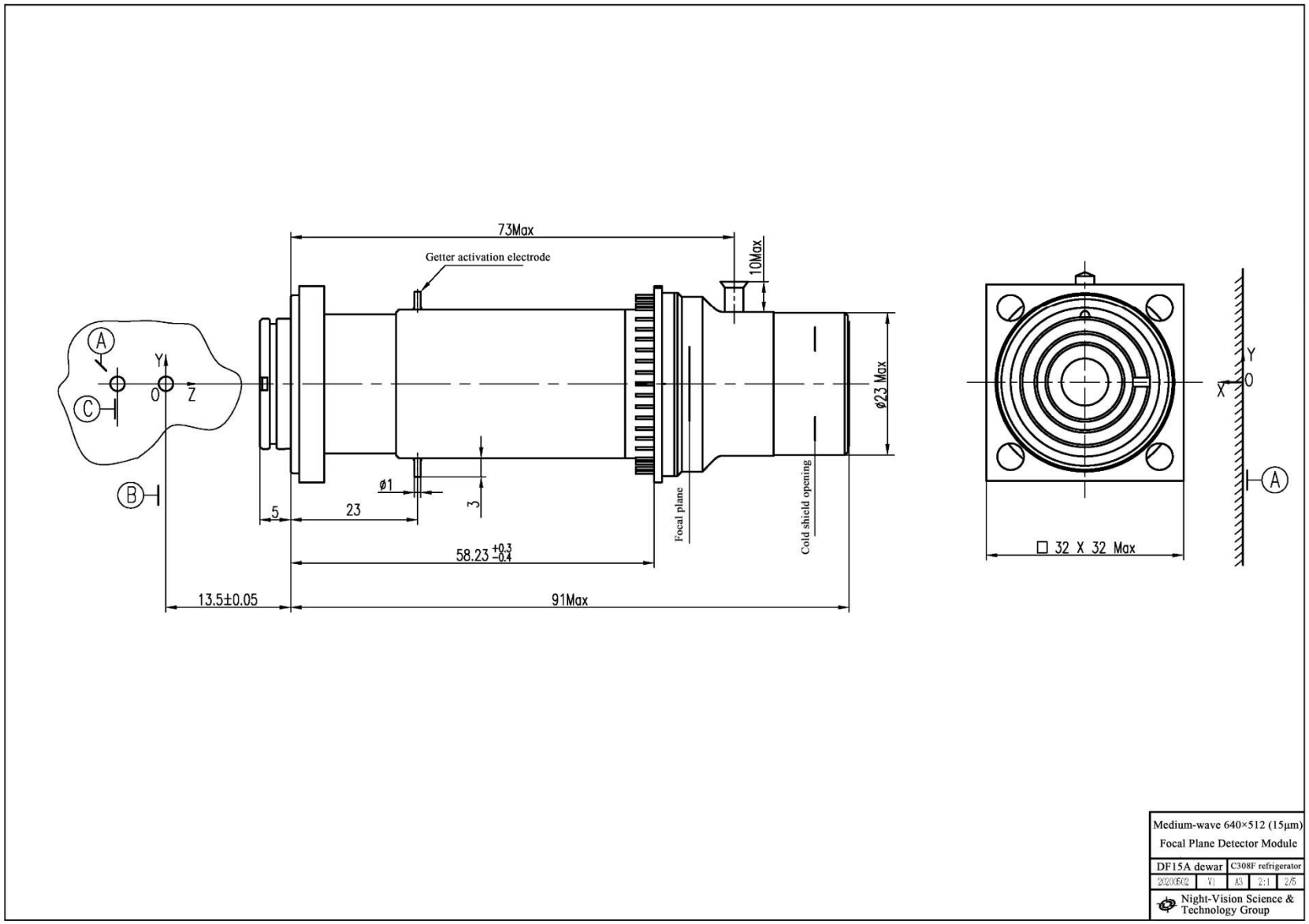
SERDAT: 34 bits (loaded between falling edge of DATAVALID and the next rising edge of INT)

Sequence: Rmin(8) Rmin(0) Rmax(8) Rmax(0) Cmin(7) Cmin(0) Cmax(7) Cmax(0)

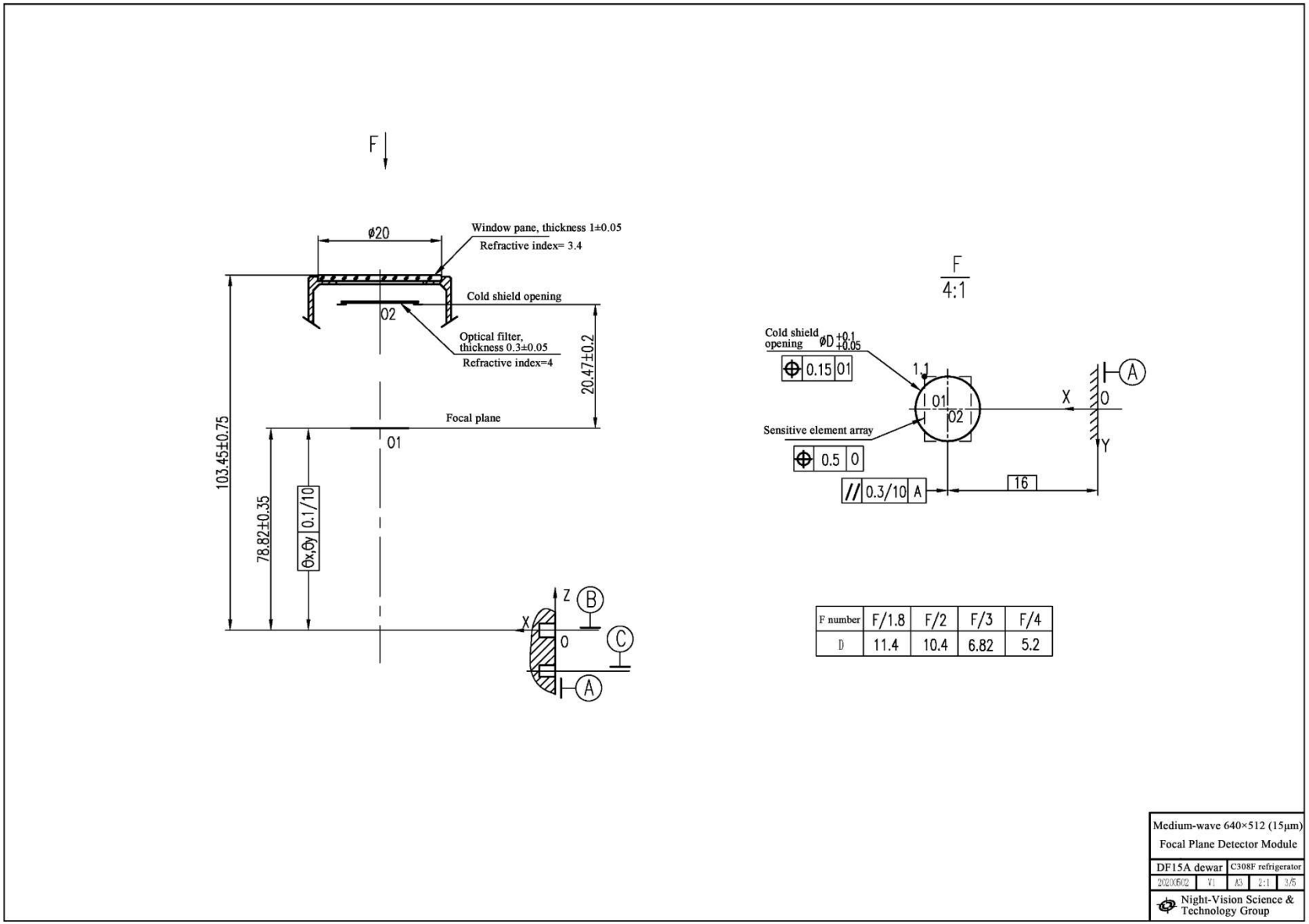
Attached Fig. 1-2 Serial Communication Waveform in 640×512 Window Mode



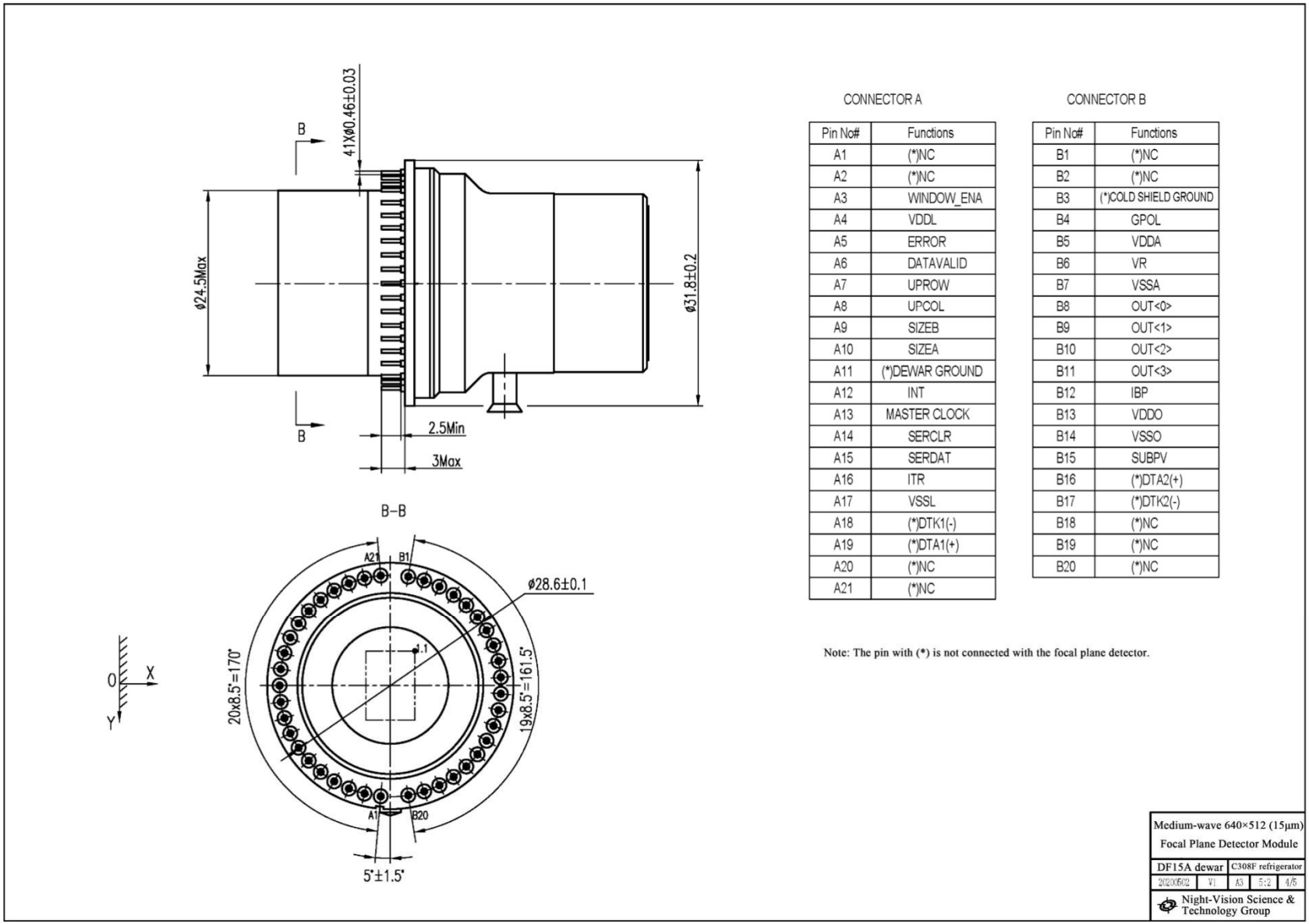
Attached Fig. 2-1 Mechanical Interface Dimension of Detector Module



Attached Fig. 2-2: Mechanical Interface Dimension of Detector Module



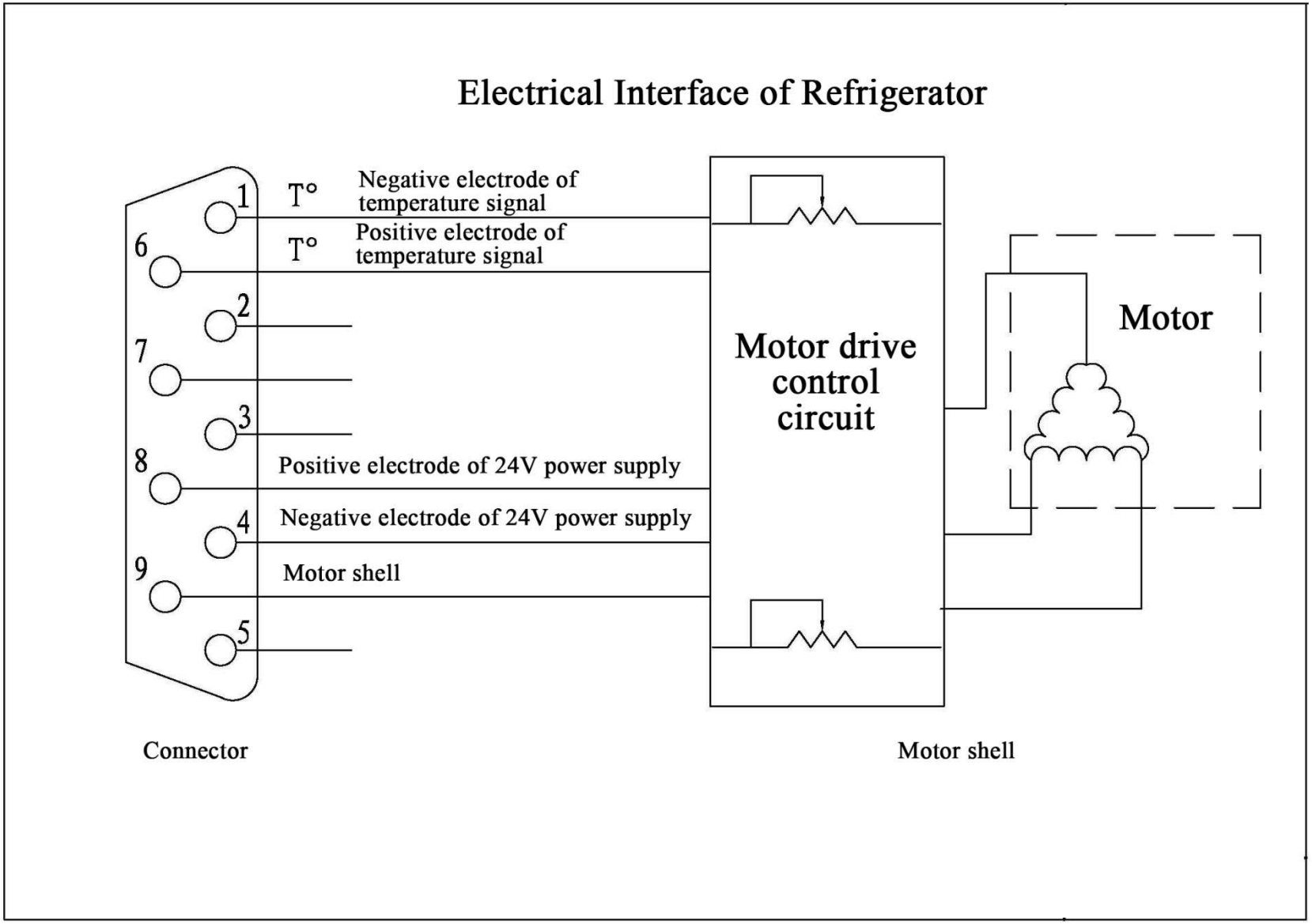
Attached Fig. 3 Optical Interface Diagram of Detector Module (F1.8/2/3/4)



Pin No#	Functions
A1	(*)NC
A2	(*)NC
A3	WINDOW_ENA
A4	VDDL
A5	ERROR
A6	DATAVALID
A7	UPROW
A8	UPCOL
A9	SIZEB
A10	SIZEA
A11	(*)DEWAR GROUND
A12	INT
A13	MASTER CLOCK
A14	SERCLR
A15	SERDAT
A16	ITR
A17	VSSL
A18	(*)DTK1(-)
A19	(*)DTA1(+)
A20	(*)NC
A21	(*)NC

Pin No#	Functions
B1	(*)NC
B2	(*)NC
B3	(*)COLD SHIELD GROUND
B4	GPOL
B5	VDDA
B6	VR
B7	VSSA
B8	OUT<0>
B9	OUT<1>
B10	OUT<2>
B11	OUT<3>
B12	IBP
B13	VDDO
B14	VSSO
B15	SUBPV
B16	(*)DTA2(+)
B17	(*)DTK2(-)
B18	(*)NC
B19	(*)NC
B20	(*)NC

Attached Fig. 4 Electrical Interface Diagram of Detector Module



Attached Fig. 5: Electrical Interface Diagram of Cooler Controller